**What Is Claimed Is:**

1. A method for amplifying capacitively coupled inter-chip communication signals, comprising:

receiving an input signal at a capacitive receiver pad from a capacitive transmitter pad;

amplifying the input signal through one or more cascaded CMOS inverter stages; and

periodically initializing the input voltage of the first CMOS inverter stage, wherein the initialization involves:

suspending data transmission on the capacitive transmitter pad and setting the voltage on the capacitive transmitter pad to a middle point between a voltage that represents logic "1" and a voltage that represents logic "0";

coupling the output of the first CMOS inverter stage to its input, thereby equilibrating the input voltage of the first CMOS inverter to a switching-threshold of the first CMOS inverter stage when the capacitive transmitter pad is at the middle point between the voltage that represents logic "1" and the voltage that represents logic "0", and thereby allowing a small input signal voltage swing to trigger an amplified output signal voltage swing; and

after the input voltage of the first CMOS inverter stage substantially stabilizes at the switching threshold, uncoupling the output of the first CMOS inverter stage from the input of the first CMOS inverter

stage and then resuming data transmission on the capacitive transmitter pad.

2. The method of claim 1, wherein coupling the output of the first CMOS inverter stage to its input involves coupling its output to its input through a switch, which is turned on during the initialization and then turned off before the middle-point voltage on the capacitive transmitter pad is replaced by data.

3. The method of claim 2, wherein the switch comprises one of an NMOS transistor, a PMOS transistor, and a CMOS switch.

4. The method of claim 1, wherein the preferred number of CMOS inverter stages is the minimum number satisfying inequality $[(V_{PHIGH} - V_{PLOW}) - n \cdot |V_{TP}| - n \cdot |V_{TN}|] \leq \mathbf{v_{in}}$, where

$n$ is the number of CMOS inverter stages;

$V_{PHIGH}$ is the high power supply voltage;

$V_{PLOW}$ is the low power supply voltage;

$V_{TP}$ is the turn-on threshold voltage of a PMOS transistor that comprises a CMOS inverter;

$V_{TN}$ is the turn-on threshold voltage of a NMOS transistor that comprises a CMOS inverter; and

$\mathbf{v_{in}}$ is the peak-to-peak swing of the input signal received from the capacitive receiver pad.

5. The method of claim 4, wherein

the PMOS source voltage of each CMOS inverter stage is equal to or higher than the PMOS source voltage of its immediately preceding CMOS inverter stage; and wherein

the NMOS source voltage of each CMOS inverter stage is equal to or lower than the NMOS source voltage of its immediately preceding CMOS inverter stage.

6. The method of claim 5, wherein

obtaining the PMOS source voltage of each CMOS inverter stage involves coupling a number of diode-connected PMOS transistors in series between the high power supply voltage and the PMOS source of each CMOS inverter; and wherein

obtaining the NMOS source voltage of each CMOS inverter stage involves coupling a number of diode connected NMOS transistors in series between the low power supply voltage and the NMOS source of each CMOS inverter.

7. The method of claim 5, wherein the PMOS source voltage and NMOS source voltage of each CMOS inverter stage are $[V_{PHIGH} - (n - i)\cdot|V_{TP}|]$ Volts and $[V_{PLOW} + (n - i)\cdot|V_{TN}|]$ Volts, respectively, where $i = 1, 2, \ldots n$ is the index of each stage, and where the index of the first stage is 1 and the index of the last stage is $n$.

8. The method of claim 7, wherein

obtaining the PMOS source voltage of each CMOS inverter stage involves coupling $(n - i)$ diode-connected PMOS transistors in series between the high

power supply voltage and the PMOS source of each CMOS inverter according to each stage's index *i*; and wherein

obtaining the NMOS source voltage of each CMOS inverter stage involves coupling $(n - i)$ diode-connected NMOS transistors in series between the low power supply voltage and the NMOS source of each CMOS inverter according to each stage's index *i*.

9. The method of claim 1, further comprising reducing current flow through the second or subsequent stage during initialization, and fixing the output of the second or subsequent stage to a high or low voltage sufficient to turn off a PMOS transistor or an NMOS transistor in the next stage during initialization.

10. An apparatus that amplifies capacitively coupled inter-chip communication signals, comprising:

a capacitive transmitter pad configured to transmit a signal;

a capacitive receiver pad configured to receive an input signal;

one or more cascaded CMOS inverter stages configured to amplify the input signal;

an initialization mechanism configured to periodically initialize the input voltage of the first CMOS inverter stage, wherein the initialization mechanism is also configured to,

suspend data transmission on the capacitive transmitter pad and set the voltage on the capacitive transmitter pad to a middle point between a voltage that represents logic "1" and a voltage that represents logic "0",

couple the output of the first CMOS inverter stage to its input, thereby equilibrating the input voltage of the first CMOS inverter to a

switching-threshold of the first CMOS inverter stage when the capacitive transmitter pad is at the middle point between the voltage that represents logic “1” and the voltage that represents logic “0”, and thereby allowing a small input signal voltage swing to trigger an amplified output signal voltage swing; and

after the input voltage of the first CMOS inverter stage substantially stabilizes at the switching threshold, uncouple the output of the first CMOS inverter stage from the input of the first CMOS inverter stage and then resuming data transmission on the capacitive transmitter pad.

11. The apparatus of claim 10, wherein the output of the first CMOS inverter stage is coupled to its input through a switch, which is turned on during the initialization and then turned off before the middle-point voltage on the capacitive transmitter pad is replaced by data.

12. The apparatus of claim 11, wherein the switch comprises one of an NMOS transistor, a PMOS transistor, and a CMOS switch.

13. The apparatus of claim 10, wherein the preferred number of CMOS inverter stages is the minimum number satisfying inequality $[(V_{PHIGH} - V_{PLOW}) - n\cdot|V_{TP}| - n\cdot|V_{TN}|] \leq v_{in}$, where

$n$ is the number of CMOS inverter stages;

$V_{PHIGH}$ is the high power supply voltage;

$V_{PLOW}$ is the low power supply voltage;

$V_{TP}$ is the turn-on threshold voltage of a PMOS transistor that comprises a CMOS inverter;

$V_{TN}$ is the turn-on threshold voltage of a NMOS transistor that comprises a CMOS inverter; and

$v_{in}$ is the peak-to-peak swing of the input signal received from the capacitive receiver pad.

14. The apparatus of claim 13, wherein

the PMOS source voltage of each CMOS inverter stage is equal to or higher than the PMOS source voltage of its immediately preceding CMOS inverter stage; and wherein

the NMOS source voltage of each CMOS inverter stage is equal to or lower than the NMOS source voltage of its immediately preceding CMOS inverter stage.

15. The apparatus of claim 14, wherein

a number of diode-connected PMOS transistors are coupled in series between the high power supply voltage and the PMOS source of each CMOS inverter; and wherein

a number of diode-connected NMOS transistors are coupled in series between the low power supply voltage and the NMOS source of each CMOS inverter.

16. The apparatus of claim 14, wherein the PMOS source voltage and NMOS source voltage of each CMOS inverter stage are $[V_{PHIGH} - (n - i)\cdot|V_{TP}|]$ Volts and $[V_{PLOW} + (n - i)\cdot|V_{TN}|]$ Volts, respectively, where $i = 1, 2, \ldots n$ is the

index of each stage, and where the index of the first stage is 1 and the index of the last stage is $n$.

17. The apparatus of claim 16, wherein

$(n - i)$ diode-connected PMOS transistors are coupled in series between the high power supply voltage and the PMOS source of each CMOS inverter according to each stage's index $i$; and wherein

$(n - i)$ diode-connected NMOS transistors are coupled in series between the low power supply voltage and the NMOS source of each CMOS inverter according to each stage's index $i$.

18. The apparatus of claim 10, further comprising a mechanism configured to reduce current flow through the second or subsequent stage during initialization, and to fix the output of the second or subsequent stage to a high or low voltage sufficient to turn off a PMOS transistor or an NMOS transistor in the next stage during initialization.

19. A computer system that amplifies capacitively coupled inter-chip communication signals, comprising:

a processor located on a first chip;

a memory located on a second chip;

a capacitive transmitter pad on the first or second chip configured to transmit a signal;

a capacitive receiver pad on the other of the first or the second chip configured to receive an input signal;

one or more cascaded CMOS inverter stages configured to amplify the input signal;

an initialization mechanism configured to periodically initialize the input voltage of the first CMOS inverter stage, wherein the initialization mechanism is configured to,

suspend data transmission on the capacitive transmitter pad and set the voltage on the capacitive transmitter pad to a middle point between a voltage that represents logic “1” and a voltage that represents logic “0”,

couple the output of the first CMOS inverter stage to its input, thereby equilibrating the input voltage of the first CMOS inverter to a switching threshold of the first CMOS inverter stage when the capacitive transmitter pad is at the middle point between the voltage that represents logic “1” and the voltage that represents logic “0”, and thereby allowing a small input signal voltage swing to trigger an amplified output signal voltage swing; and

after the input voltage of the first CMOS inverter stage substantially stabilizes at the switching threshold, uncouple the output of the first CMOS inverter stage from the input of the first CMOS inverter stage and then resuming data transmission on the capacitive transmitter pad.

20. The computer system of claim 19, wherein the output of the first CMOS inverter stage is coupled to its input through a switch, which is turned on during the initialization and then turned off before the middle-point voltage on the capacitive transmitter pad is replaced by data.

21. The computer system of claim 20, wherein the switch comprises one of an NMOS transistor, a PMOS transistor, and a CMOS switch.

22. The computer system of claim 19, wherein the preferred number of CMOS inverter stages is the minimum number satisfying inequality $[(V_{PHIGH} - V_{PLOW}) - n\cdot|V_{TP}| - n\cdot|V_{TN}|] \leq v_{in}$, where

$n$ is the number of CMOS inverter stages;

$V_{PHIGH}$ is the high power supply voltage;

$V_{PLOW}$ is the low power supply voltage;

$V_{TP}$ is the turn-on threshold voltage of a PMOS transistor that comprises a CMOS inverter;

$V_{TN}$ is the turn-on threshold voltage of a NMOS transistor that comprises a CMOS inverter; and

$v_{In}$ is the peak-to-peak swing of the input signal received from the capacitive receiver pad.

23. The computer system of claim 22, wherein

the PMOS source voltage of each CMOS inverter stage is equal to or higher than the PMOS source voltage of its immediately preceding CMOS inverter stage; and wherein

the NMOS source voltage of each CMOS inverter stage is equal to or lower than the NMOS source voltage of its immediately preceding CMOS inverter stage.

24. The computer system of claim 23, wherein

a number of diode-connected PMOS transistors are coupled in series between the high power supply voltage and the PMOS source of each CMOS inverter; and wherein

a number of diode-connected NMOS transistors are coupled in series between the low power supply voltage and the NMOS source of each CMOS inverter.

25. The computer system of claim 23, wherein the PMOS source voltage and NMOS source voltage of each CMOS inverter stage are $[V_{PHIGH} - (n - i)\cdot|V_{TP}|]$ Volts and $[V_{PLOW} + (n - i)\cdot|V_{TN}|]$ Volts, respectively, where $i = 1, 2, \ldots n$ is the index of each stage, and where the index of the first stage is 1 and the index of the last stage is $n$.

26. The computer system of claim 25, wherein

$(n - i)$ diode-connected PMOS transistors are coupled in series between the high power supply voltage and the PMOS source of each CMOS inverter according to each stage's index $i$; and wherein

$(n - i)$ diode-connected NMOS transistors are coupled in series between the low power supply voltage and the NMOS source of each CMOS inverter according to each stage's index $i$.

27. The computer system of claim 19, further comprising a mechanism configured to reduce current flow through the second or subsequent stage during initialization, and to fix the output of the second or subsequent stage to a high or low voltage sufficient to turn off a PMOS transistor or an NMOS transistor in the next stage during initialization.